UNIVERSITY OF TWENTE.

Exam Computer Systems/Computer Architecture and Organisation

Bachelor 2nd year, EE and CS, EWI

Module/course code: Computer Systems 201400210(CS) / 201400217(EE)
Date: XXXXXXXXXXX
Time: 8:45-10:30 *(+25% for students who may use extra time)*
Module-coördinator: A.B.J. Kokkeler
Instructor: E. Molenkamp / A.B.J. Kokkeler

Type of test: Closed book
Allowed aids during the test: Writing materials, simple calculator

27 questions on 8 pages and 4 pages with the ARC documentation

Instructions for this examination:

1. Scientific or graphical calculators, laptops, mobile phones, books etc. are not allowed. Put those in your bag now (and **switched off**)!
2. Write your answers on this paper, in the provided boxes , and hand in this exam **and** the multiple choice form (even when you did not answer any questions).
3. All multiple choice questions have exactly one correct answer; place an X in the correct box and copy the answer to the multiple choice form.
4. The multiple choice form is scanned and automatically corrected. Make sure to fill in that form completely (except for the "docent / teacher" part).
5. The multiple choice questions (weighted equally), correction for guessing is used.
6. Write your name and student number on each page of this exam
7. Furthermore fill in your name, educational programme and student number below on this page.
8. The documentation refers to the ARC processor. If a problem indicates that it is about the **subset ARC** processor then only the instructions listed in figure 5-2 (documentation page 2) may be used.

Logic symbols: **not a** is also represented as $\overline{a}$, **a'**, **!a**, **#a**
a and b is also represented as **a.b**, **a&b**
a or b is also represented as **a + b**
a xor b is also represented as $a \oplus b$

(please underline your family name (i.e., the name on your student card), so that we know how to sort))

Name: .....

Student number: .....

Educational programme (EE, TCS, ..): .....

Question 1

Which statement is true?

a☐ A DRAM memory cell is smaller than an SRAM memory cell and a DRAM memory cell needs to be refreshed

b☐ A DRAM memory cell is larger than an SRAM memory cell and a DRAM memory cell needs to be refreshed

c☐ A DRAM memory cell is smaller than an SRAM memory cell and a SRAM memory cell needs to be refreshed.

d☐ A DRAM memory cell is larger than an SRAM memory cell and a SRAM memory cell needs to be refreshed.

Question 2

A 64 bit processor uses Little-Endian addressing. The bytelanes of the databus are numbered from 0 to 7 where bytelane 0 uses datalines 0-7, bytelane 1 uses datalines 8-15 and so on. Access to memory is data-aligned and a processor writes a single byte to address 2F83H. Which bytelane carries the byte to be written into memory?

a☐ 2

b☐ 3

c☐ 5

d☐ 6

Question 3

What is correct?

a☐ In case of a decentralized bus arbitration scheme, the bus arbiter grants access to a bus via a predetermined priority scheme.

b☐ In a synchronous bus, timing is not related to a clock signal.

c☐ If a device wants to make use of the bus, an interrupt request is activated.

d☐ None of the above.

Question 4

Consider the following interrupt scenario and an interrupt **cannot** suspend other interrupts:

Task	Service time	Maximum allowed latency	Maximum Frequency
A	30 ms	500 ms	1/(2000 ms)
B	20 ms	70 ms	1/(1000 ms)
C	40 ms	35 ms	1/(500 ms)
D	5 ms	10 ms	1/(250 ms)

What is correct?

a☐ Maximum allowed latencies for all the tasks are met

b☐ Task D can prevent task A being serviced in time

c☐ Task A can prevent task D being serviced in time

d☐ Task B can prevent task C being serviced in time

Question 5

An embedded computer system has a physical address space of 4 GB. The memory is byte addressable. Memory mapped I/O is used. The system contains an Ethernet controller, video-RAM and a Wifi controller according to the following specifications concerning addressing.

Video-RAM:	1 GB at the lowest addresses of the address range.
Ethernet controller:	1 MB directly following the area for the Ethernet controller.
Wifi controller:	2 GB at the highest addresses of the address range.
Shadowing is allowed.	

The signals to select the different areas are respectively *SelVideo, SelEth* en *SelWifi*.
The bits of the address bus are $A_{N-1}..A_0$ (N is number of address lines, right most bit has index 0)

What is the minimal equation for *SelVideo* ?

a☐ *SelVideo* = $!A_{31}$ & $!A_{30}$

b☐ *SelVideo* = $!A_{32}$

c☐ *SelVideo* = $!A_{31}$

d☐ *SelVideo* = $!A_{31}$ & A_{30}

Question 6

See question 23.

What is the minimal equation for *SelEth* ?

a☐ *SelEth* = $!A_{31}$ & $!A_{30}$

b☐ *SelEth* = $!A_{32}$

c☐ *SelEth* = $!A_{31}$

d☐ *SelEth* = $!A_{31}$ & A_{30}

Question 7

A 16-bits microprocessor has an on-chip primary cache with the following characteristics:

Address space:	8 MB, Byte-addressing
Primary cache:	Size: 128 KB (excluding tags)
	Slotsize: 64 B
	Organisation: 8-way set-associative

For the primary cache, a byte-address is split into parts that are used for, respectively, comparison with the *tag* in the cache, selection of a *set in the cache*, selection of a *word in a slot* and selection of a *byte in a word*. Note: the right most bit has number 0.

What are the bit numbers of the address that selects **set in the cache**?

a☐ 12, 11, 10, 9, 8, 7, 6

b☐ 13, 12, 11, 10, 9, 8

c☐ 13, 12, 11, 10, 9, 8, 7, 6

d☐ 14, 13, 12, 11, 10, 9, 8, 7

Question 8

See question 25

What are the bit numbers of the address that selects **word in slot**?

a☐ 5, 4, 3, 2, 1

b☐ 4, 3, 2, 1, 0

c☐ 6, 5, 4, 3, 2

d☐ none of the above

Question 9

A dynamic RAM chip is organised as follows: 128 x 2 bits. Using multiple of these chips, a memory module of in total 2 Kbytes has to be built. The word width is 32 bits.
How many columns (to establish the correct word width) and how many rows does the memory module contain?

a☐ columns: 16 rows: 4

b☐ columns: 32 rows: 4

c☐ columns: 32 rows: 2

d☐ columns: 16 rows: 2