

## CAO Reading guide weeks 1 and 2, version 1

Week 1	
<p>Tuesday/Wednesday Lectures 8:45-10:30</p>	<p><b>Murdocca, Appendix A1 until A.15 and A.17</b></p> <p>A.4.1: Technology details is informative for TI-students (EE-students are familiar with these details). Dominant technology is CMOS. CMOS configurations for three gates are shown in figure A-12. (An AND gate is realized as a NAND gate with a NOT gate! → Hence an AND gate is larger and slower than a NAND gate)</p> <p>A.5: Note: the DeMorgan's Theorem is often used!</p> <p>A.7: Not for TI-students (for EE-students it is part of "Digital Hardware")</p> <p>A.8: Skip this section</p> <p>A.9: Skip this section</p> <p>A.10.6: Only the principle of the Ripple-Carry Adder (example A-1). For EE-students programmable logic is part of "Digital Hardware".</p> <p>A.11: Instead of this chapter I prefer reading:  <a href="http://faculty.lasierra.edu/~ehwang/digitaldesign/index.html">http://faculty.lasierra.edu/~ehwang/digitaldesign/index.html</a> [accessed 20 August 2018]  chapter 6 (latches and flipflops) chapter 6.1 until 6.11 (not 6.7.1 and figure 6.14c).  TI students can skip VHDL, for EE students it is part of the "Digital Hardware"</p> <p><b>The definition used in this course:</b>  <b>A latch is a LEVEL-SENSITIVE device and a flip-flop is an EDGE-TRIGGERED device.</b></p> <p>In this course the behavior of these devices are important. You must know the behavior of:</p> <ul style="list-style-type: none"> <li>• SR-latch</li> <li>• D-latch (DE-latch)</li> <li>• D-flipflop</li> <li>• DE-flipflop</li> </ul> <p>For EE students also (part of "digital hardware"):</p> <ul style="list-style-type: none"> <li>• T-flipflop</li> <li>• SR-flipflop</li> <li>• JK-flipflop</li> </ul> <p>A.17.3: Not part of this course</p> <p>A.17.4: Informative for TI-students (for EE students it is part of the "Digital Hardware")</p>
<p>Friday Lecture 8.45-10.30</p>	<p>Do you have questions? If no questions than a short meeting.</p>

Friday Lecture 13:45-15:30	<b>Murdocca, chapter 2.1, 2.2 and 2.4</b> (number representation) - 2.2 Floating point format <u>only</u> for base 2. - 2.4 Informative
Week 2	
Monday Lecture 8:45-10:30	<b>Murdocca, chapter 3</b> - Skip the “ripple borrow subtractor” (fig. 3-4 and fig 3-5). (Figure 3-6 is used for addition and subtraction.) - skip 3.2.2 (unsigned division) - skip 3.2.3 (signed division) - skip 3.3 FP arithmetic is for EE students; part of “Digital Hardware” - skip 3.4.1 not TI students; High performance addition is for EE students part of “Digital Hardware” - skip 3.4.2 not TI students; Booth algorithm for EE students (“Digital Hardware”) - skip 3.4.3 - skip 3.4.4
Tuesday Lecture 8:45-10:30	<b>Murdocca, chapter 4</b> The focus is on the instruction set architecture of the ARC processor. You can download the ARCTools ( <a href="http://iisatech.com/murdocca/CAO/Tools.html">http://iisatech.com/murdocca/CAO/Tools.html</a> ); use mirror site. You must be able to write simple assembly programs (and you can simulate these programs).  - skip pages 121-123 “ Control instructions: software traps”. Interrupts, and more, (these subject are handled in weeks 3 and 4). - skip 4.9 not part of this course
Wednesday Lecture 8:45-10:30	<b>Murdocca, chapter 5</b> - 5.1 - 5.2 (It is sufficient if you know the behavior of the ALU operations, not the implementation details. Not for exam the details on page 156-160) - 5.3 skip 5.3.1 (we use a synchronous sequential circuit approach) skip 5.3.3 skip 5.3.4 skip 5.4 skip 5.5 skip 5.6
Friday Lecture 8:45-10:30	Do you have questions? If no questions than a short meeting.
Friday Lecture 13:45-15:30	No new theory. If on schedule no lecture.
Week 3	
Monday Lecture 8:45-10:30	<b>Diagnostic Test</b>