Homework Lecture 2

1. Exercise A.28

"**changes from 0 to 1**" should be interpreted as the "in previous clock cycle the input was 0 (at active edge of clock) and the current input value is 1". (Mealy FSM)

2. Exercise A.29

"last three bits" where the last bit is the current input value (Mealy FSM).

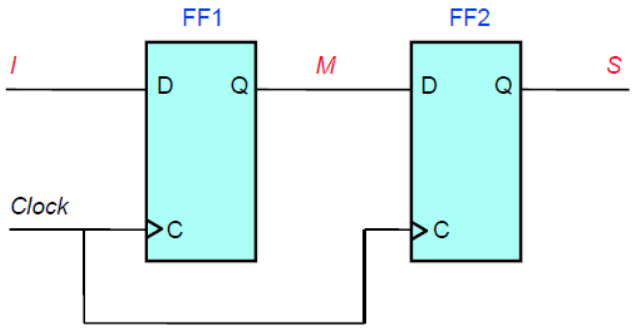
3. Exercise A.36

4. Exercise A37

(only SOP-form)

5. Exercise A.38

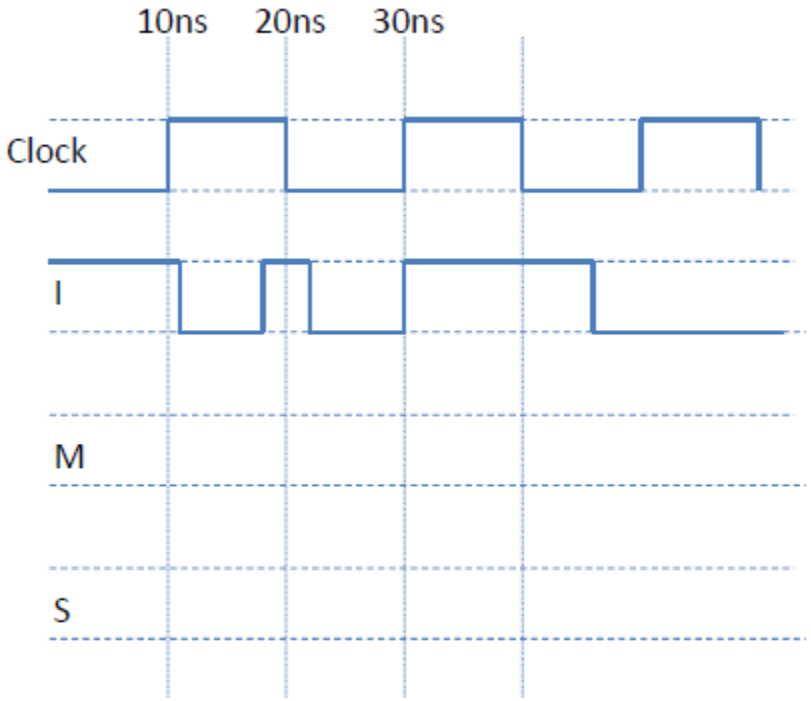
6. Exercise: 2 FF's in series



The timing properties of both flip-flops are: Tsu = 6 ns, Th = -2 ns, Tco = 3 ns;

The wires have a delay of 0 ns.

Draw the waveform for M and S (we assume ideal edges; instantaneously from 0→1 and 1→0). At 0 ns M and S are both 0.

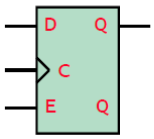


7. Exercise: realize a DE flipflop

DE flip-flop

° DE flip-flop is D flip-flop with enable **E**; when **E=0** flip-flop output is unchanged. When **E=1** flip-flop behaves as D flip-flop

E	D	Q+	
0	0	Q	Unchanged
0	1	Q	Unchanged
1	0	0	Reset
1	1	1	Set



Realize the DE flip-flop with a D flip-flop and combinational logic.