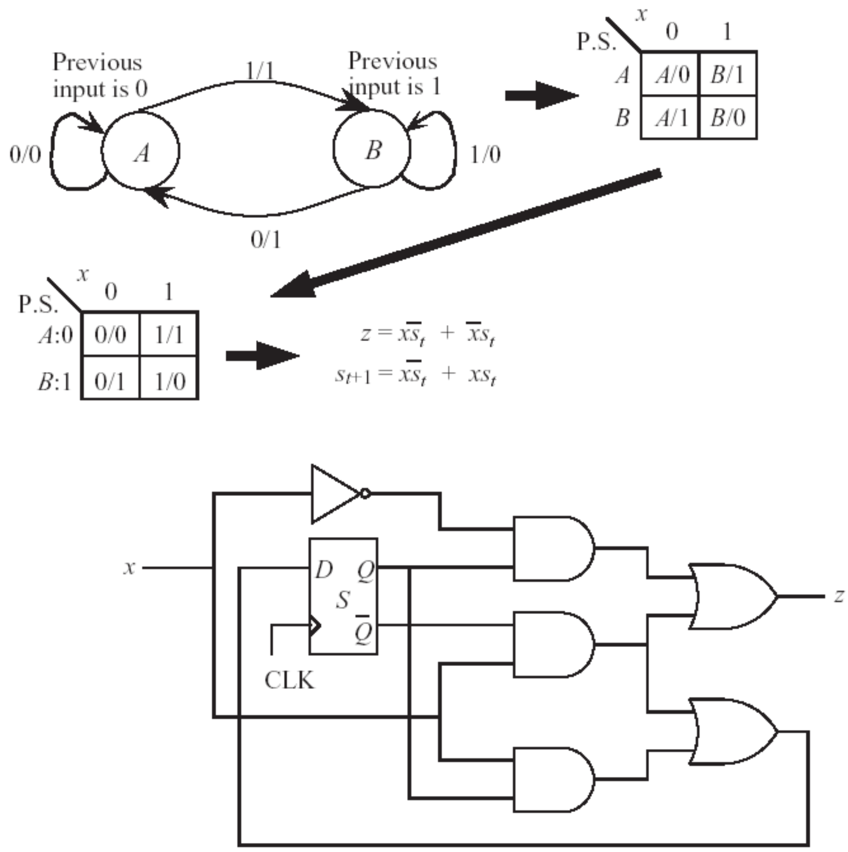
Homework Lecture 2 (solutions)

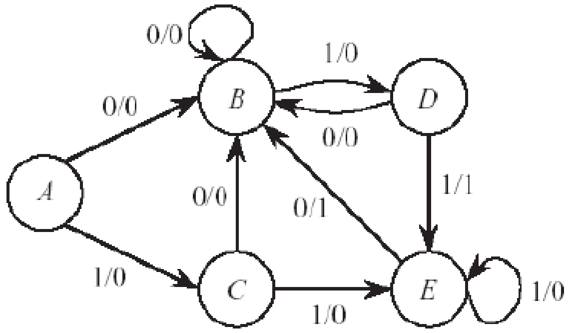
1. Exercise A.28



This is the solution of the author. My comment:

- Instead of $z = x\overline{s_t} + \bar{x}s_t$ write $= x \cdot \overline{s_t} + \bar{x} \cdot s_t$
- S_{t+1} is not minimal. Minimum SOP-form is S_{t+1} =x

2. Exercise A.29

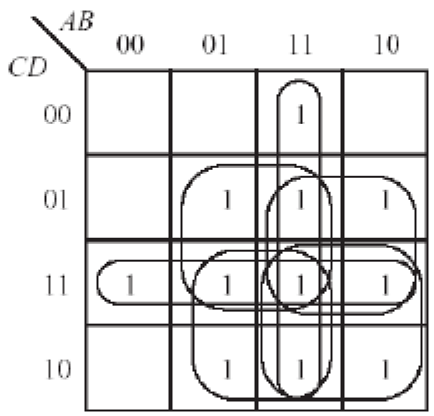


Meanings of States	
A	No inputs seen yet
B	Seen '0'
C	Seen '1'
D	Seen '01'
E	Seen '11'

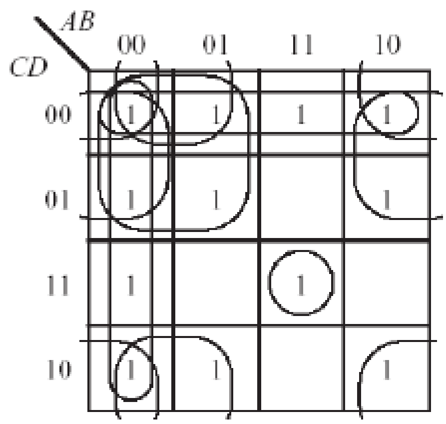
P.S. \ Input	X = 0	X = 1
A	*B*/0	*C*/0
B	*B*/0	*D*/0
C	*B*/0	*E*/0
D	*B*/0	*E*/1
E	*B*/1	*E*/0

I would have used meaningful names for the states, e.g. S0 (zero detected), S1, S01 (zero followed by 1 detected) and S11.

3. Exercise A.36

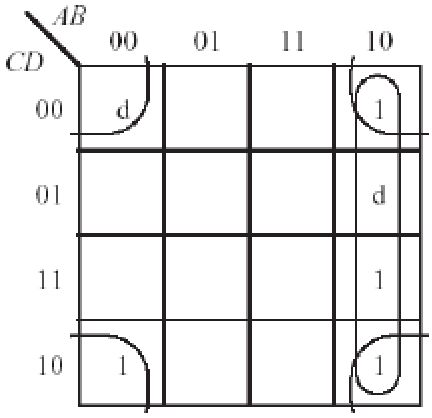


$f(A,B,C,D) = AB + CD + BD + AD + BC + AC$



$g(A,B,C,D) = ABCD + \bar{B}\bar{D} + \bar{C}\bar{D} + \bar{A}\bar{B} + \bar{A}\bar{D} + \bar{A}\bar{C} + \bar{B}\bar{C}$

4. Exercise A.37

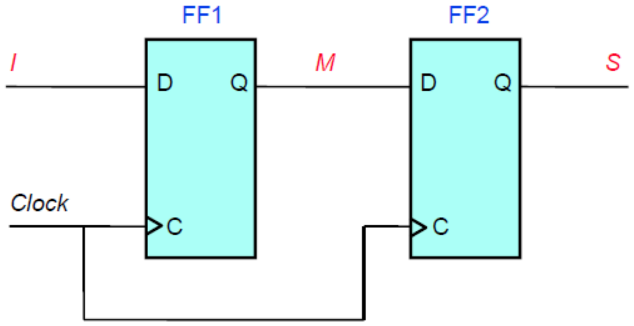


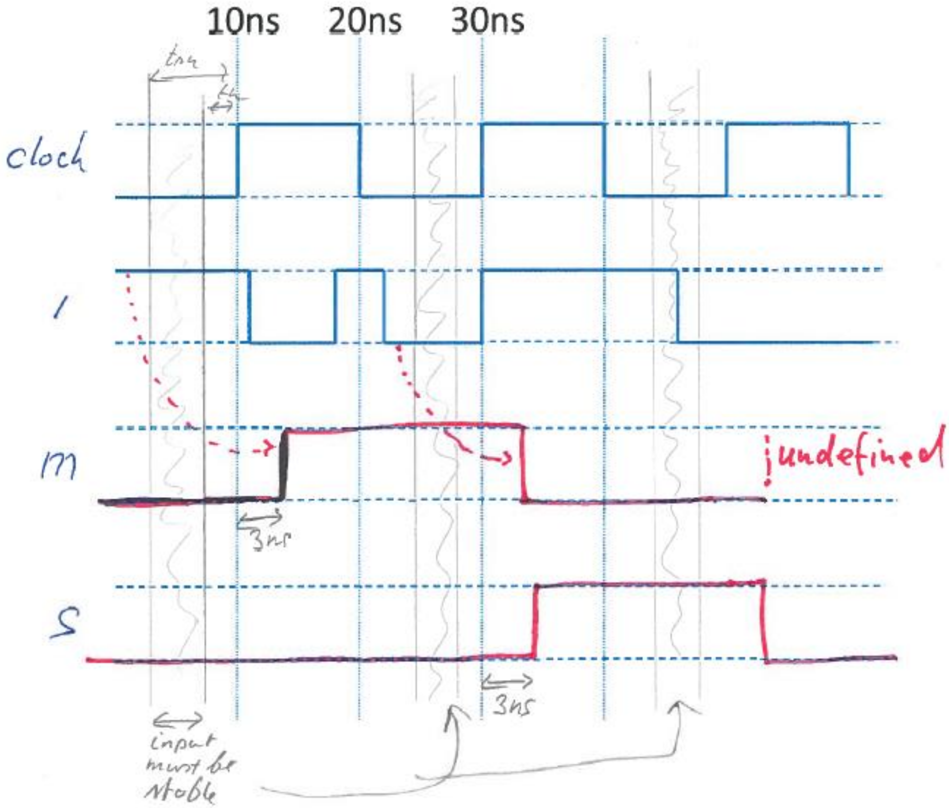
SOP Form: $f(A,B,C,D) = A\bar{B} + \bar{B}\bar{D}$

5. Exercise A.38

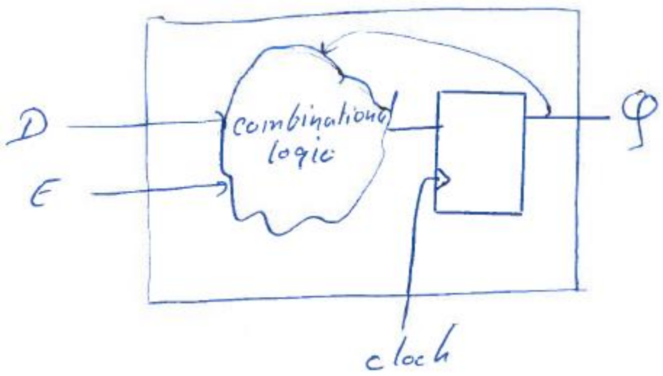
No. The don’t cares are used during the design process. Once the design is fixed, the don’t cares are either 0 or 1.

6. Exercise: 2 FF’s in series





7. Exercise: realize a DE flip-flop



Function table DE flip-flop

E	D	Q+
0	0	Q
0	1	Q
1	0	0
1	1	1

The combinational logic has as inputs: Q, D and E and the output is connected to the input of the D flip-flop.

Q	E	D	Q+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Behavior of D flip-flop: if Q should be 1 after the next clock cycle the data input must be 1, if Q should be 0 after the next clock cycle the data input must be 0. Hence:

Q	E	D	Q+	DQ
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

DQ is input of flip flop Q

Karnaugh-map

Q \ ED	00	01	11	10
0	0	0	1	0
1	1	1	1	0

The minimal SOP-form for the combinational logic is:

$DQ = Q \cdot \bar{E} + E \cdot D$