

Errata Computer Architecture and Organization; an Integrated Approach Murdocca and Heuring

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Chapter 4:

- Section 4.2.3, pg. 105. “The lab_3 ... respectively”. Reference is made to a ‘lab_3’ label in figure 4.8 but this figure does not contain such a label. Besides that, the sentence is correct. In the next paragraph of the same section, reference is made to a ‘left-pointing arrow’ in figure 4.8. This can also not be found in the figure.
- Section 4.2.4, pg. 111, last paragraph. ‘Register ... right by nine bit positions..’ should be ‘Register ... right by 23 positions...’.

Chapter 6:

- Section 6.1.4, pg. 202. The section about pointers is not clear. Look at the sheets for a more precise description of pointers and their usage.

Chapter 7

- Section 7.3, pg. 255, second paragraph. Refresh cycles are mentioned but have not been explained. Look at the sheets.
- Section 7.5.1, pg. 267, first paragraph. Memory interleaving has been mentioned in section 7.3 but not explained.
- Section 7.5.6, pg 278. The formulas for H_2 and T_{EFF} are not correct. The correct formulas are:

$$H_2 = \frac{\text{No. times accessed word is in L2 cache}}{\text{No. times accessed word is not in L1 cache}}$$

$$T_{EFF} = ((\text{No. L1 cache hits})(\text{L1 cache hit time}) + (\text{No. L2 cache hits})(\text{L2 cache hit time}) + (\text{No. L2 cache misses})(\text{L2 cache miss time})) / \text{Total Number of memory accesses}$$

Furthermore, the example is not elaborated correctly. This is corrected in the sheets, as they are presented during the lectures:

Multi-level Cache Memory

As an example, consider a two-level cache in which the L1 hit time is 5 ns, the L2 hit time is 20 ns, and the L2 miss time is 100 ns. There are 10,000 memory references of which 10 cause L2 misses and 90 cause L1 misses. Compute the hit ratios of the L1 and L2 caches and the overall effective access time.

H_1 is the ratio of the number of times the accessed word is in the L1 cache to the total number of memory accesses. There are a total of ~~85~~⁹⁰ (L1) and ~~15~~¹⁰ (L2) misses, and so:

$$H_1 = \frac{(10,000 - \cancel{10} - 90) \text{ hits}}{10,000 \text{ accesses}} = 99\%$$

(Continued on next slide.)

Multi-level Cache Memory (Cont')

H_2 is the ratio of the number of times the accessed word is in the L2 cache to the number of times the L2 cache is accessed, and so:

$$H_2 = \frac{\cancel{100}^{\cancel{90}} - 10 \text{ hits}}{100 \text{ accesses}} = 90\%$$

The effective access time is then:

$$\begin{aligned} T_{EFF} &= (\cancel{10,000}^{\cancel{90}} - \cancel{10} - 90 \text{ L1 hits})(5 \text{ ns per L1 hit}) + \\ &\quad (\cancel{100} - 10 \text{ L2 hits})(20 \text{ ns per L2 hit}) + \\ &\quad (10 \text{ L2 cache misses})(100 \text{ ns per L2 cache miss}) \\ &\quad / 10,000 \text{ accesses} \\ &= 5.23 \text{ ns per access} \end{aligned}$$

Chapter 8

- Section 8.4.7, pg 320. Fifth line of this section says: “.. During the falling edge of the second”. This should be: “.. During the falling edge of the first”.