Hand-in assignments (Thursday, week 1)

Your name and student number must be on each page.

Exercise 1

Simplify the following Boolean functions by means of a four-variable map (minimum SOP form):

a) F(A,B,C,D) = ∑m(1,5,9,12,13,15)

b) F(A,B,C,D) = ∑m(1,3,9,11,12,13,14,15)

c) F(A,B,C,D) = ∑m(0,2,4,5,6,7,8,10,13,15)

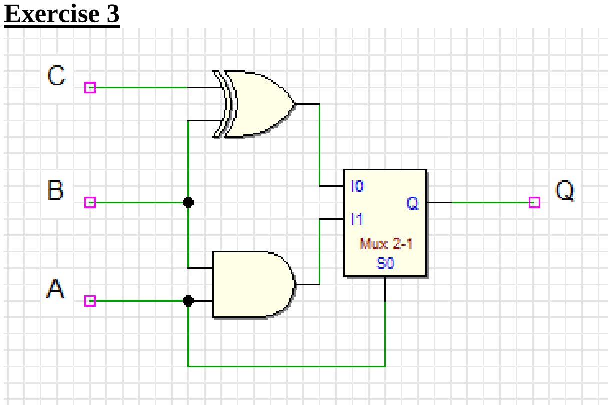
Exercise 2

Simplify the following Boolean functions in Sum-of-Products (SOP)

a) F(A,B,C,D) = ∑m(0,2) and d = ∑m(8,10,11,15)

b) F(A,B,C,D) = ∑m(7,9,13,14) and d = ∑m(0,2,5,6,8,10,11,15)

Exercise 3

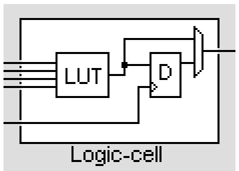


Give a minimum Boolean equation in SOP-form of this system.

Exercise 4

http://www.fpga4fun.com/FPGAinfo2.html

FPGAs are built from one basic "logic-cell", duplicated hundreds or thousands of time. A logic-cell is basically a small lookup table ("LUT"), a D flip-flop and a 2-to-1 mux (to bypass the flip-flop if desired).



The LUT is like a small RAM that can implement any logic function. It has typically a few inputs (4 in the drawing above), so for example an AND gate with 3 inputs, whose result is then OR-ed with another input would fit in one 4-input LUT.

This exercise is about the LUT (so ignore D flip-flop and multiplexer). The LUT is a memory in this example has 4 address lines (left of the LUT), and each memory address has 1 bit (so a “16×1 bit memory”).

In programmable hardware you can fill this memory during programming of the device. The lines to program the LUT are not shown in the picture. E.g. if you fill the memory with all zero’s except address 15 is 1 than it behaves like and AND gate with 4 inputs. Since only when all 4 address lines are 1 the output is 1 (only at that address a 1 is stored in the memory). All the others input combinations result in selecting a memory cell that contains a 0.

How many different combination functions can be implement with a LUT with 4 address lines and 1 output bit?

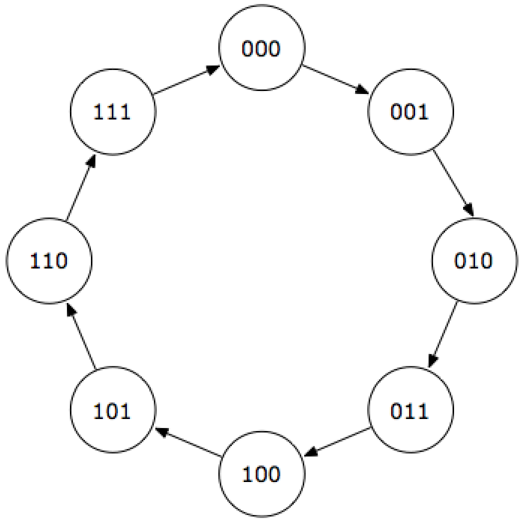
Exercise 5

A majority function has an output value of 1 if there are more ones than zeros on its inputs else the output is 0. Design a three-input majority function.

Exercise 6

Draw a schematic of a 3-to-8 decoder with enable using only NOR and NOT gates. The inputs are A2, A1, AO and E (enable). The outputs are D7..D0. When enable is 0 all outputs are 0.

Exercise 7



Given an FSM with 8 states. This is a synchronous counter. The system has no inputs (except the clock input). At each active edge it goes to the next state. The systems is realized with 3 D flip-flops, Q_2, Q_1 and Q_0. (De flip-flop outputs are also the outputs of the systems).

Determine the Boolean equations for the combinational logic for the data inputs of these flip-flops.

Exercise 8

Design a synchronous MOORE system with 1-bit input *I* and 1-bit output *Y*. The system also has a clock (*CLK*) and asynchronous low active reset input (*RST_N*).

The output *Y* is for the duration of one clock period 1when the input *I* is 1 at the rising edge of the *CLK* and at the previous rising edge of the *CLK* the input was 0.

Note: it is assumed that a change of the input does not violate the setup and hold conditions of the flip-flops.

a) Draw an FSM for this system (using meaningful names for the states!).

b) D flip-flops and binary encoding for the states are used. Determine the Boolean equations (SOP-form) for the combinational logic (input of D flip-flops and output). (You must derive this from the FSM.)

c) Draw the schematic